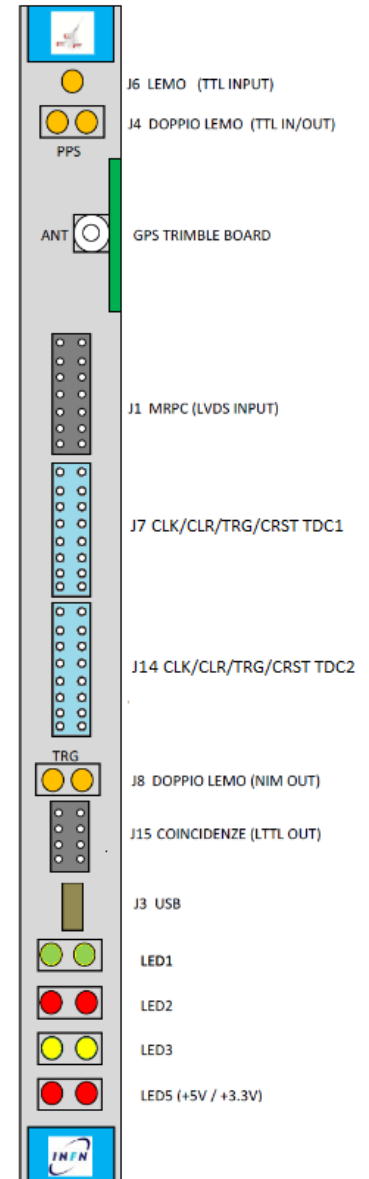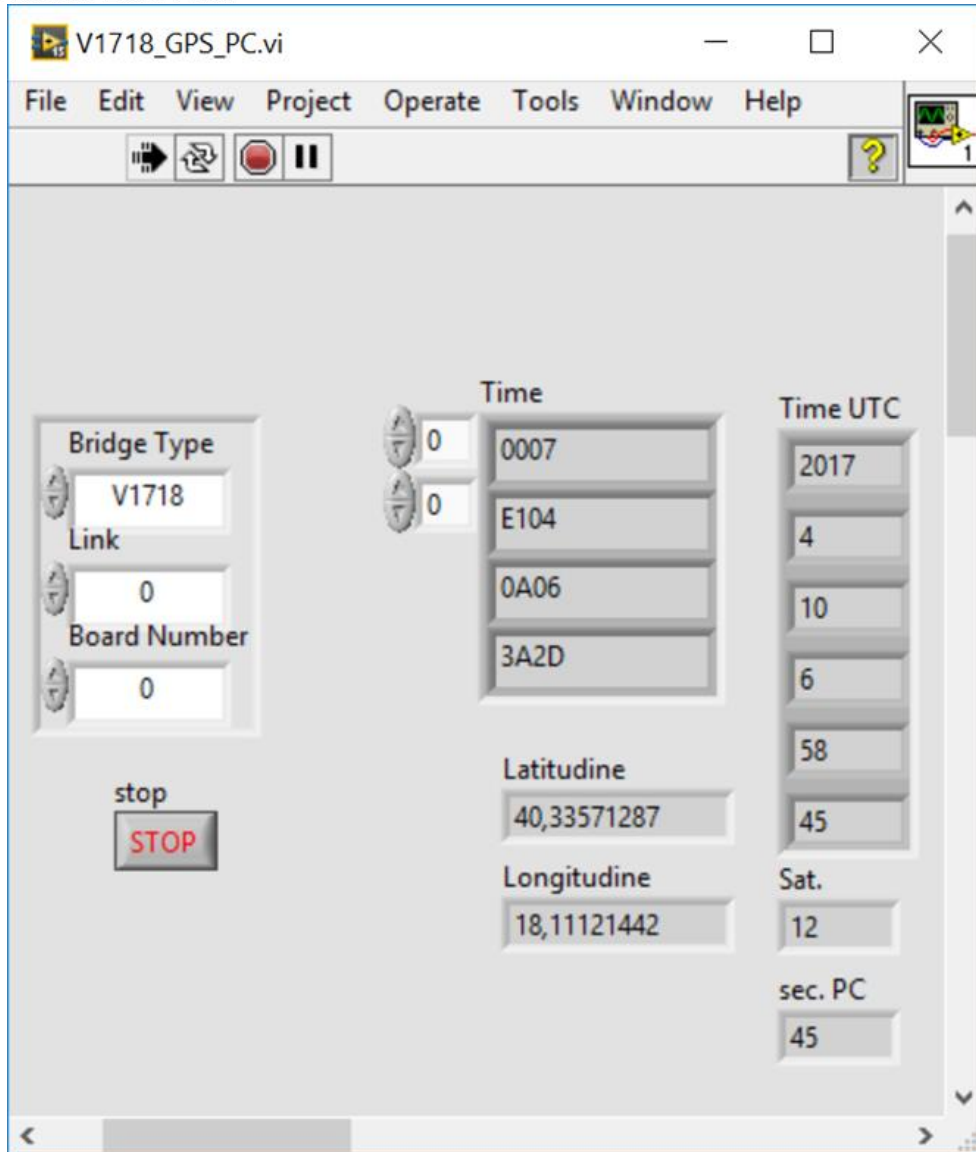# Status of the GPS-Trigger Board V.2

A. Corvaglia

Outlook

- VME GPS/Trigger board debugging status
  - Timing
  - Position
- Trigger and GPS functionality implemented
- Debugging plan

J6 LEMO (TTL INPUT)
J4 DOPPIO LEMO (TTL IN/OUT)
PPS
ANT — GPS TRIMBLE BOARD
J1 MRPC (LVDS INPUT)
J7 CLK/CLR/TRG/CRST TDC1
J14 CLK/CLR/TRG/CRST TDC2
TRG
J8 DOPPIO LEMO (NIM OUT)
J15 COINCIDENZE (LTTL OUT)
J3 USB
LED1
LED2
LED3
LED5 (+5V / +3.3V)

- **Time**
  - A shift of one second was found between PPS signal and the correlated data information. This error was fixed by a reconstruction of the calendar implemented into the FPGA
  - The choice between UTC time and GPS time is now implemented into GPS engine board (we use the UTC time for EEE)

- **Position**
  - For default the engine GPS freeze the surveyed position information (latitude/longitude) to the average value after 2k acquisition from the first start. This procedure allow a better accuracy on the time data. We decided to maintain this working condition.
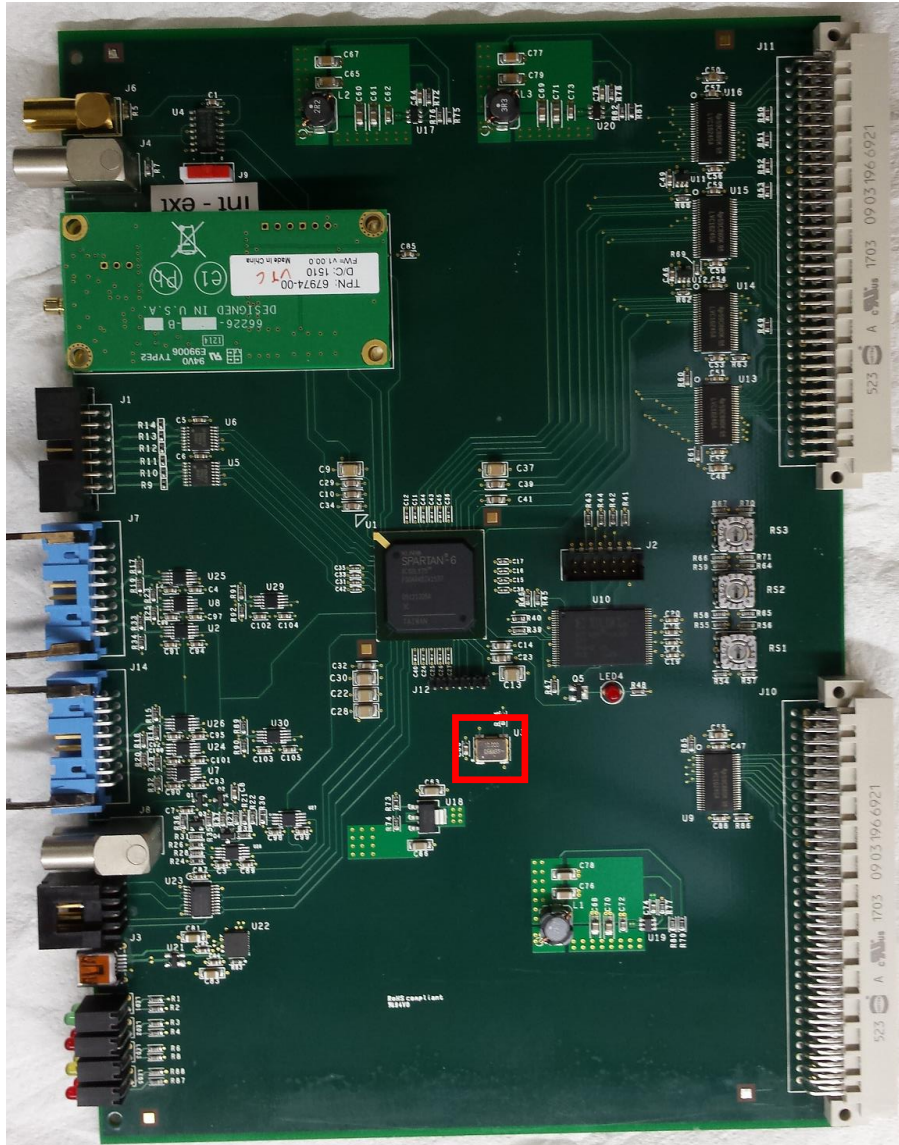
- **Trigger + clock distribution**
  - Now the trigger section can work even without the engine GPS module (in this condition the time accuracy is limited on the precision of the oscillator on the board)

- **GPS Setup**
  - For default, the setup of the engine GPS board should made through a dedicated external board. This procedure complicates the installation and the replacement of the engine GPS
  - Now the setup of the engine GPS board in made by the FPGA on the same VME board. A code implemented on the FPGA (now under test) configures and saves the data on the flash memory of the engine GPS.

Summay

- Avallabile:
  - 7 VME GPS/trigger boards
  - 4 engine GPS boards
- 5 trigger boards (no GPS functionality implemented yet) will be available for the end of next week (please let me know the addresses to send them)
  - Next we will need to get back them to install the GPS firmware on the FPGA
- GPS firmware debugging is estimate in about 2 weeks