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Status of the GPS-Trigger Board V.2

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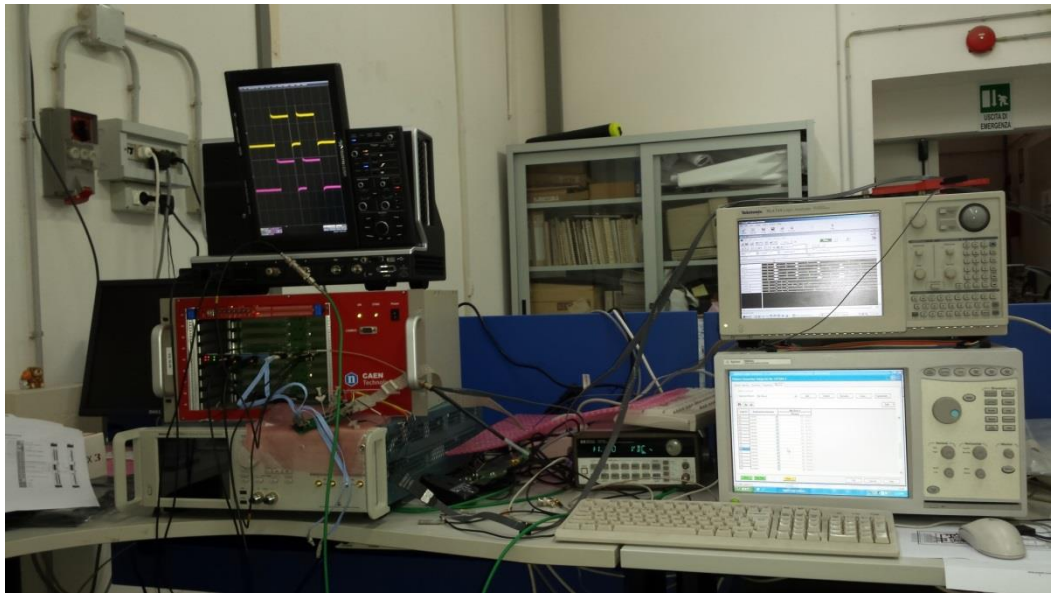
Outlook

- Differences between V.1 and V.2 GPS-Trigger board
- Signals integrity test
- Tests of data transfer on VME bus



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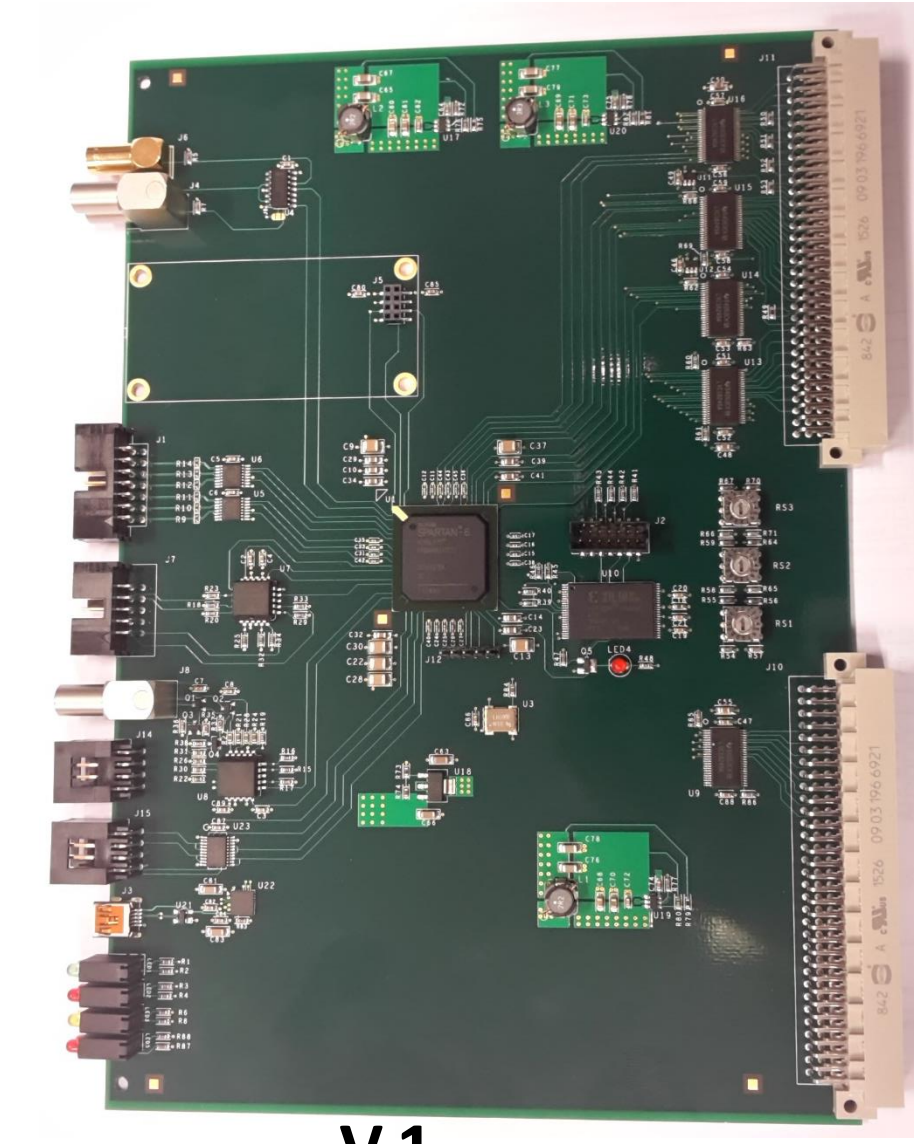
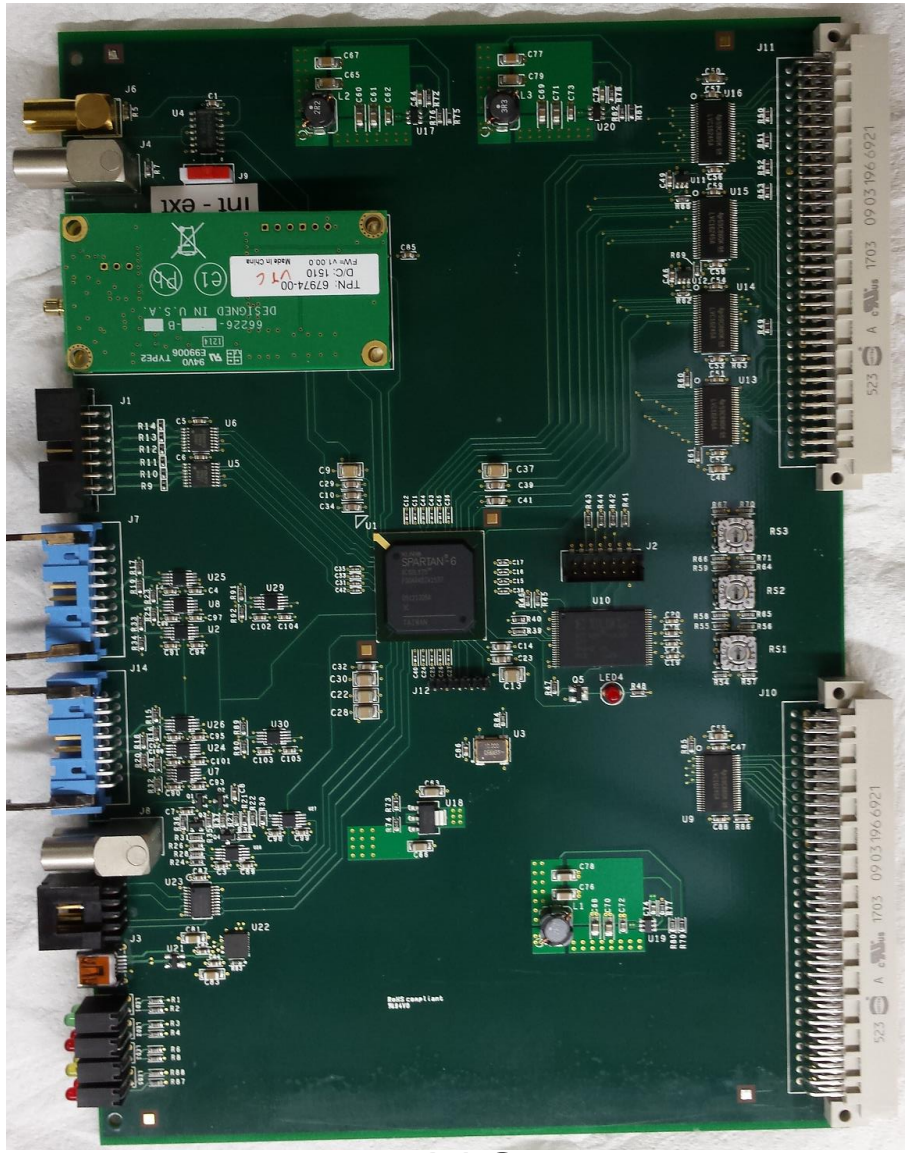
Board V.1 vs. V.2



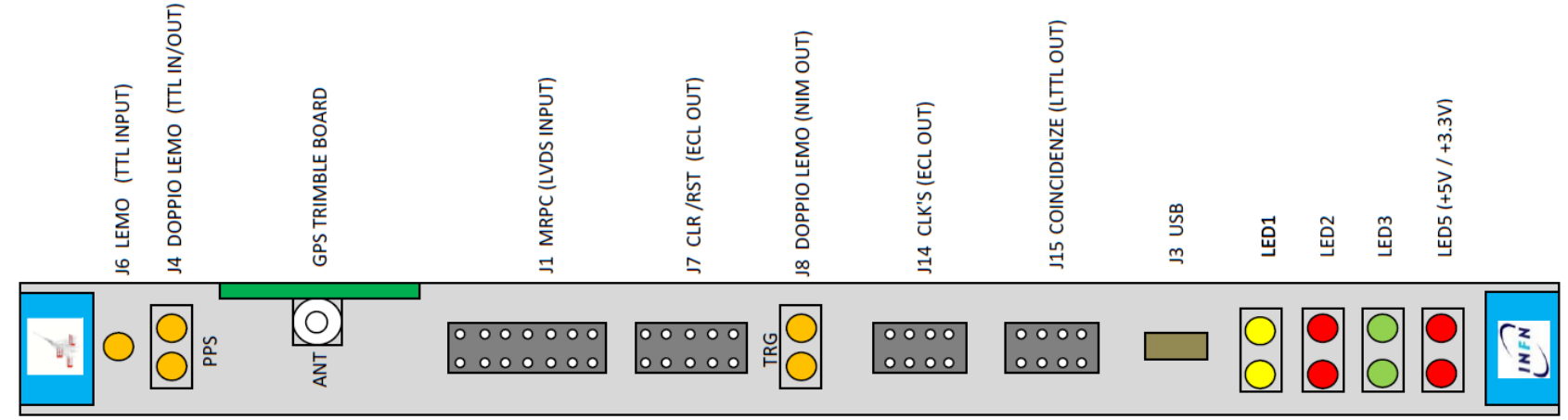
V.1

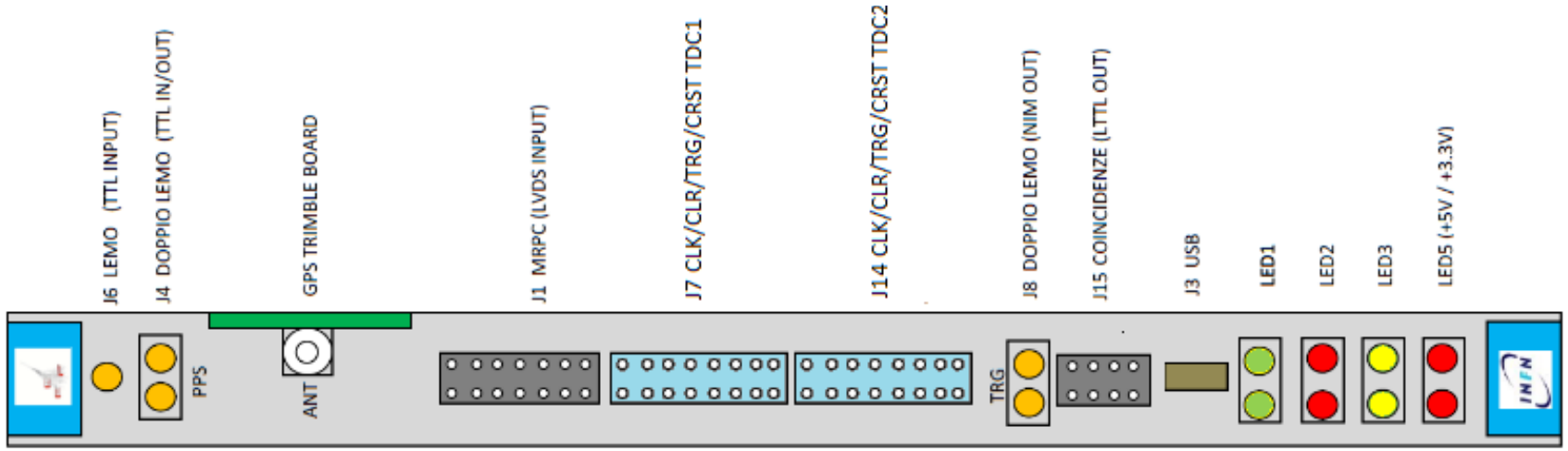
V.2 Arrived at
March 23rd , 2017

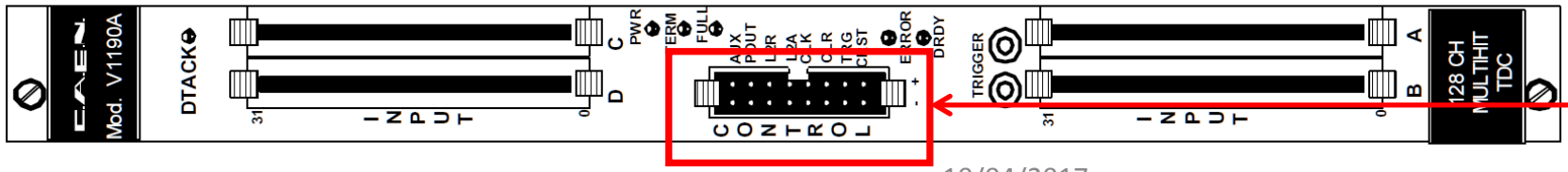


V.2

Board V.1 vs. V.2







Board V. 1 :

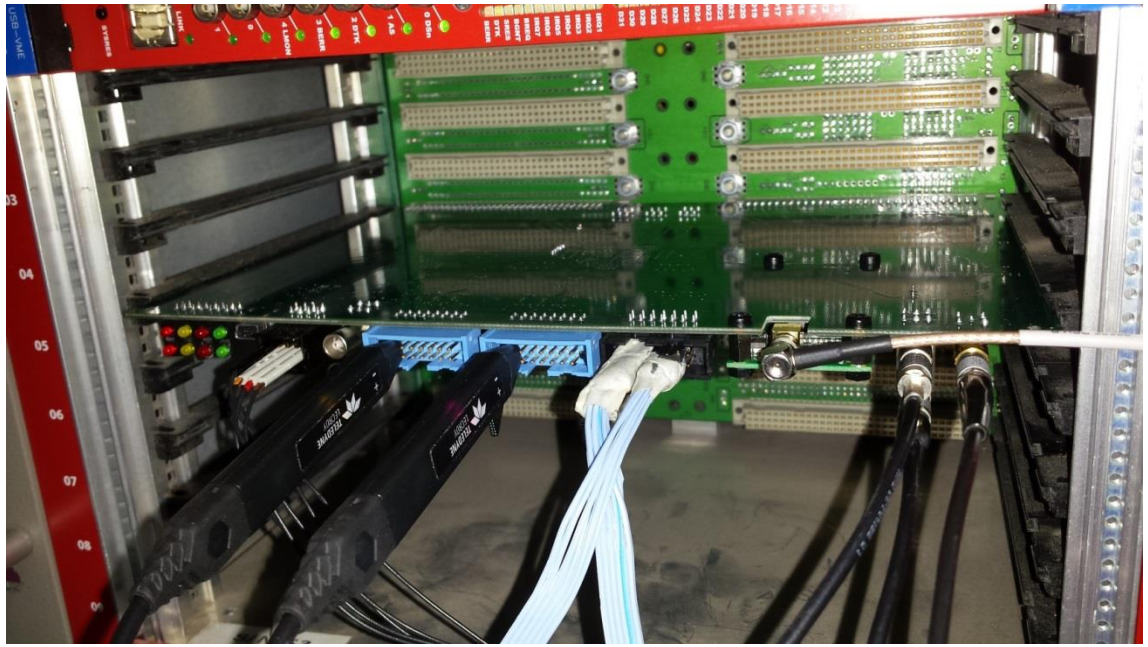
- J1 MRPC
- J7 CLRS/RST
- J14 CLK
- J8 Trigger

Board V.2

- J1 MRPC
- J7/J14 connectors full compatible with CONTROL port of TDC (CRST/TRG/CLR/CLK)

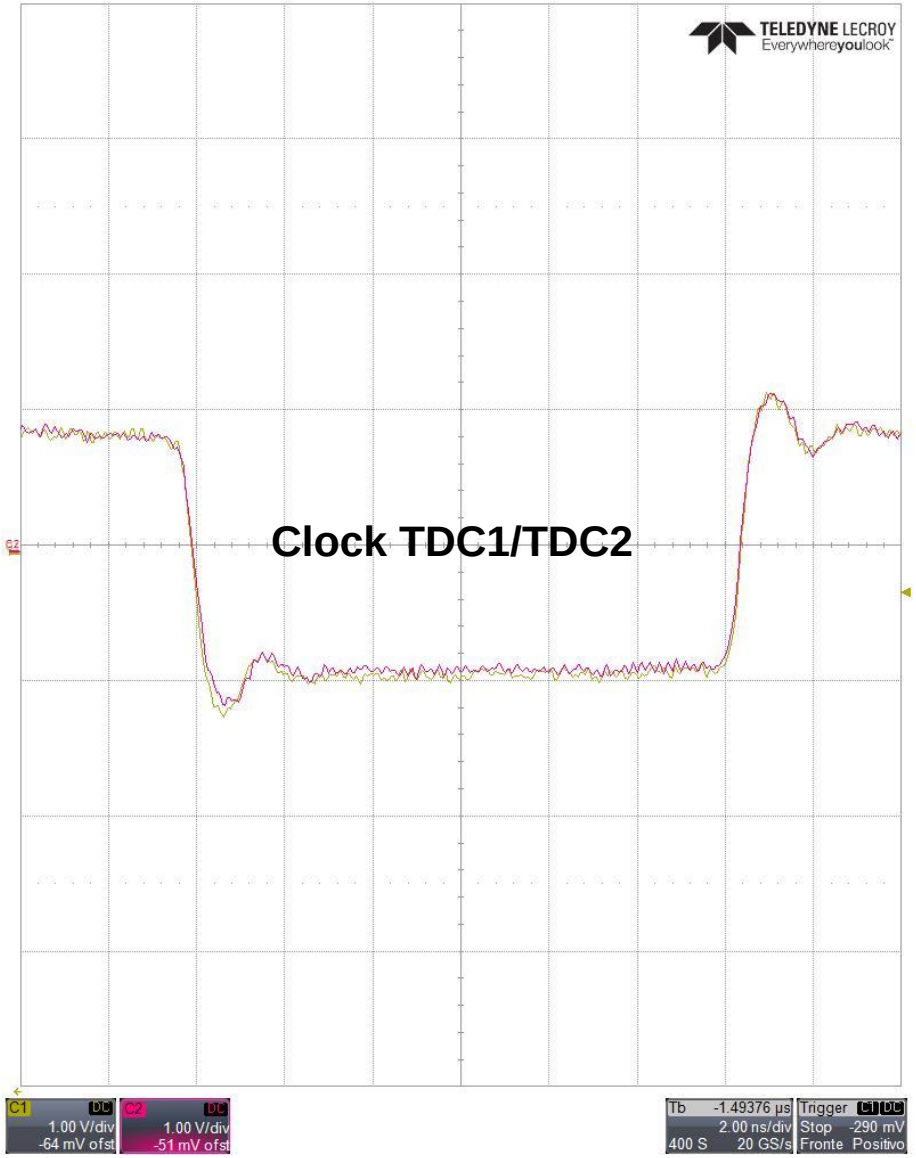
0dsn-CLR

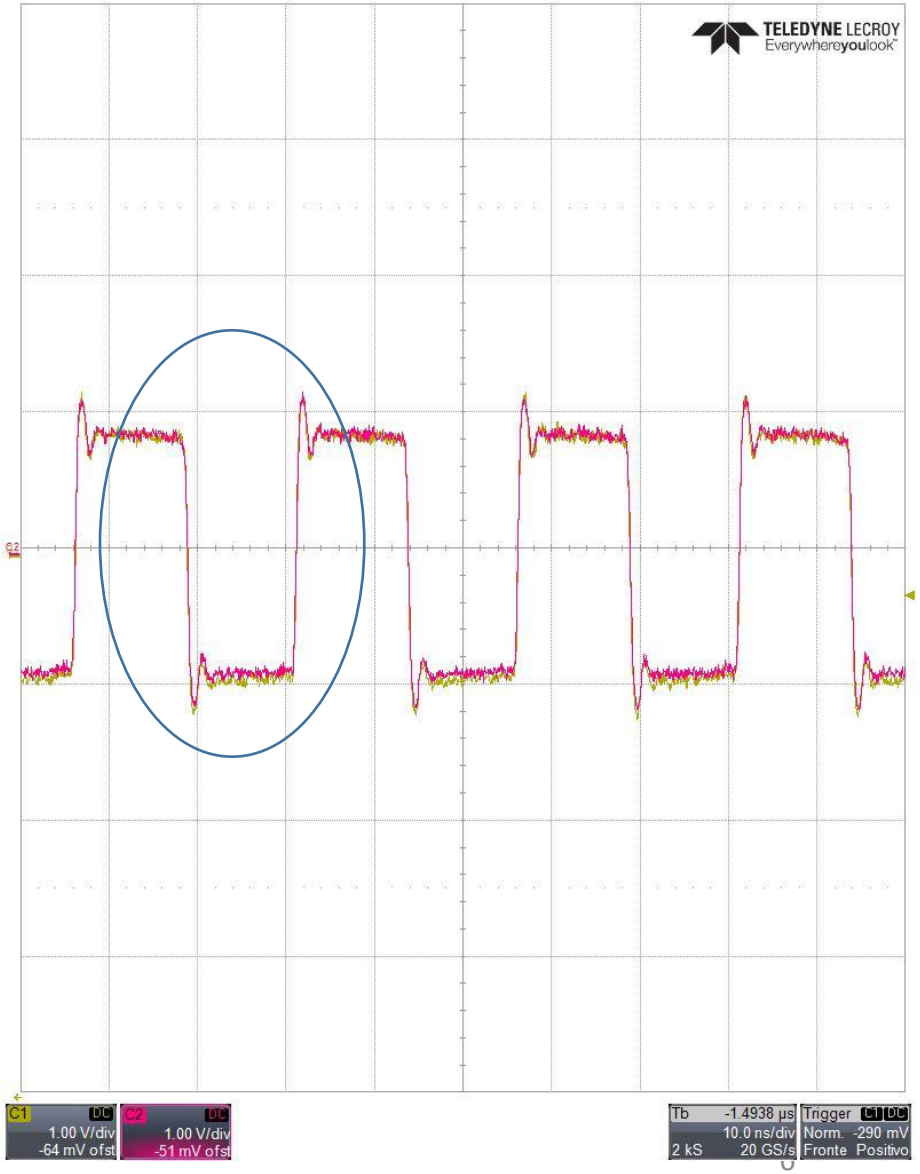
Test 1:
IN 0dsn (bridge) TTL → Out CLR (TDC1/2) ECL



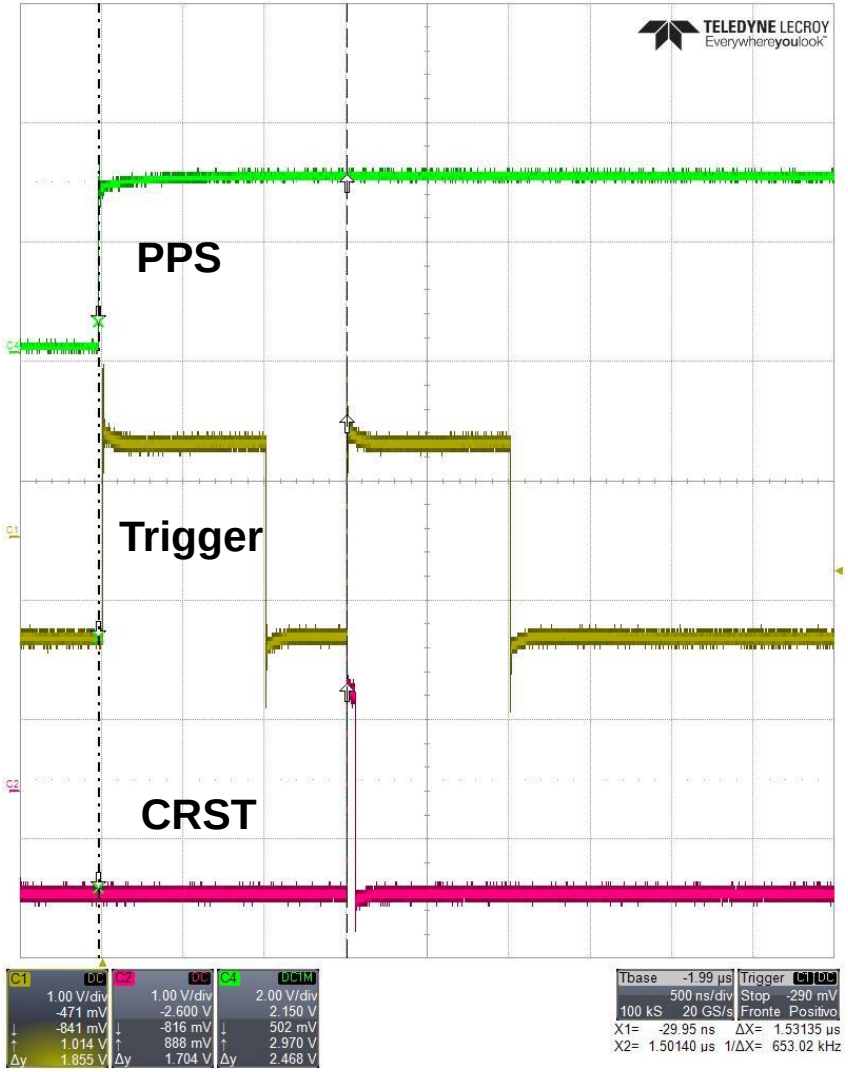
CLOCK

Test 2 :
CLK 40 MHz (TDC1/2) ECL





PPS Trigger CRST

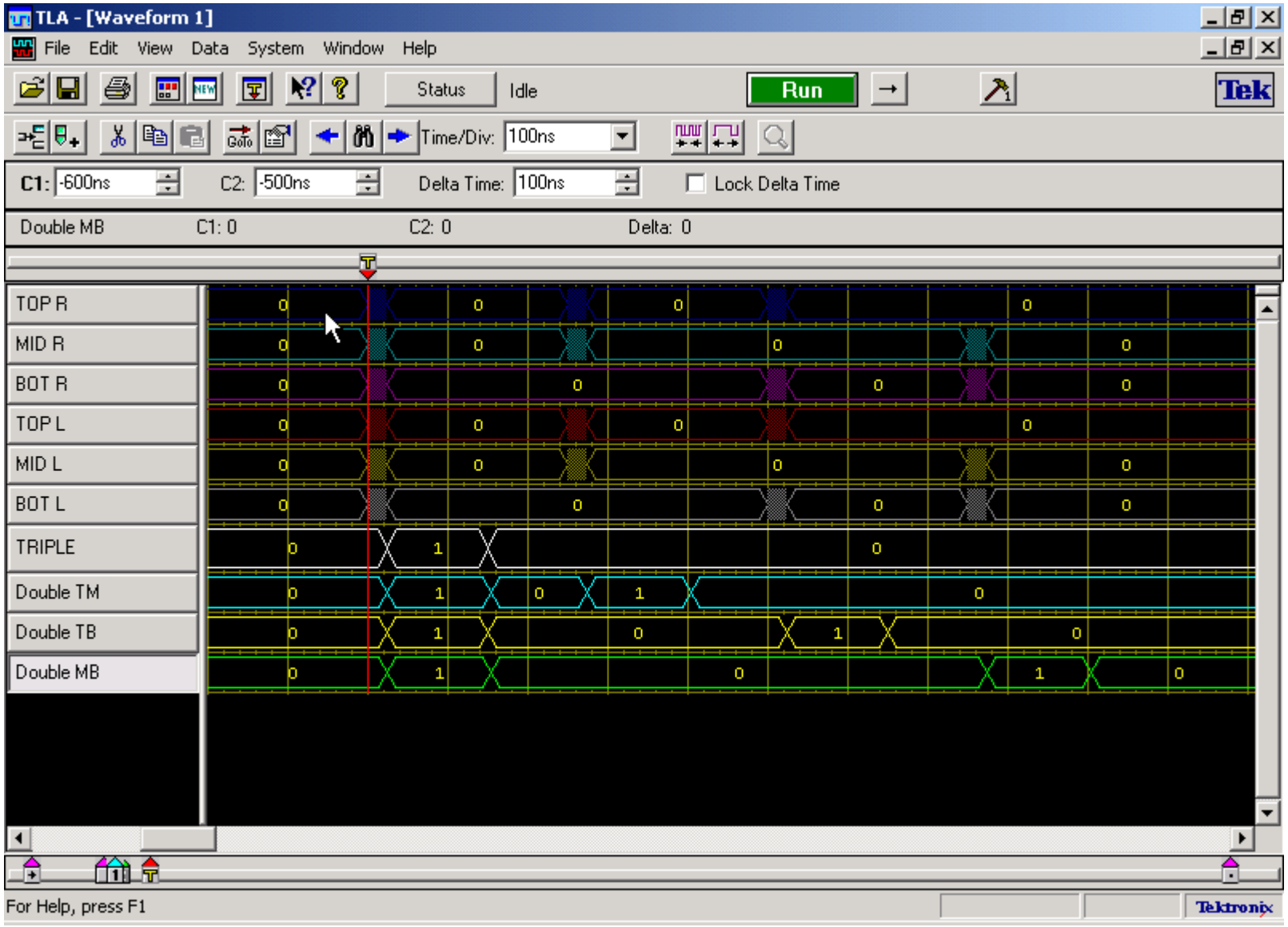


Test 3:

-IN PPS (GPS Int/Ext) TTL → Out Trigger (TDC1/2) ECL

-IN PPS (GPS Int/Ext) TTL → 1.5µs delay → Out CRST (TDC1/2) ECL

MRPC Trigger

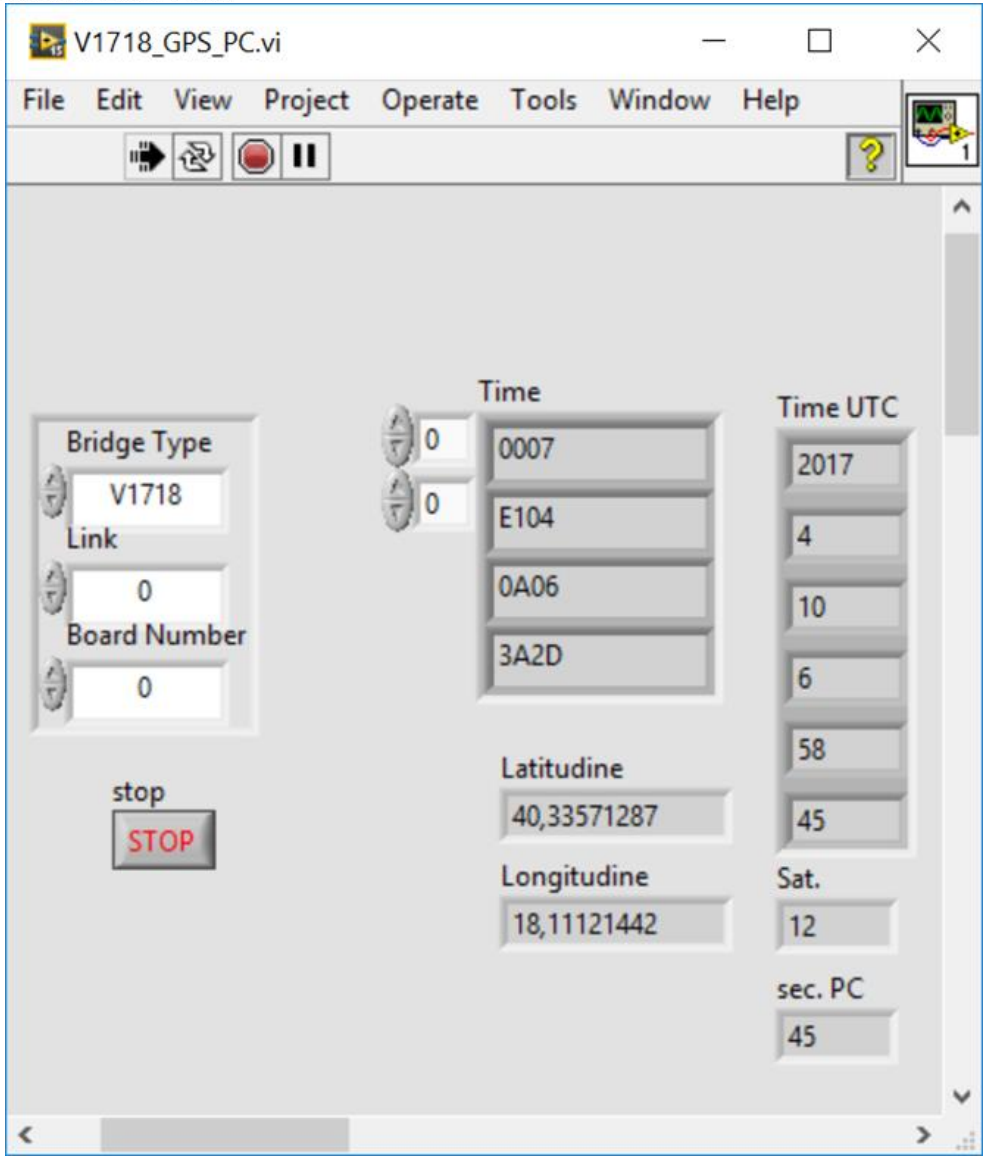


Test 4:

-IN MRPC (triple) → Out Trigger (TDC1/2) ECL

-IN MRPC (double TM-TB-MB) → Out J15 LTTL

VME BUS test



After 7.5 hours of data acquisition (~27000 events)

- **Time**
  - 0 errors of seconds
- **Position**
  - Latitude/longitude differences between subsequent measurements $<10^{-4}$ degrees (according to GSP standard)

Conclusions

- Tests given good results

- Tests to be done
  - Noise Immunity
  - Acquisition with EEE DAQ